High Efficient Power Conversion from Car Batteries to Next Generation Microcontroller Systems (PwrSwipe)

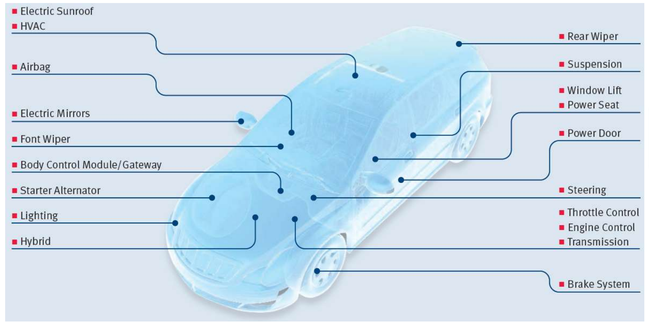
Gerhard Maderbacher[1], Karlheinz Kogler[1], Joachim Pichler[1], Federico Capponi[1], Herbert Gruber[1], Sylvia Michaelis[1], Dietrich Michaelis[1], Andreas Einwanger[2], Christoph Sandner[1], Anamaria Anca[1], Gottfried Beer[2]

[1]Infineon Technologies Austria AG - Villach, [2]Infineon Technologies AG - Regensburg

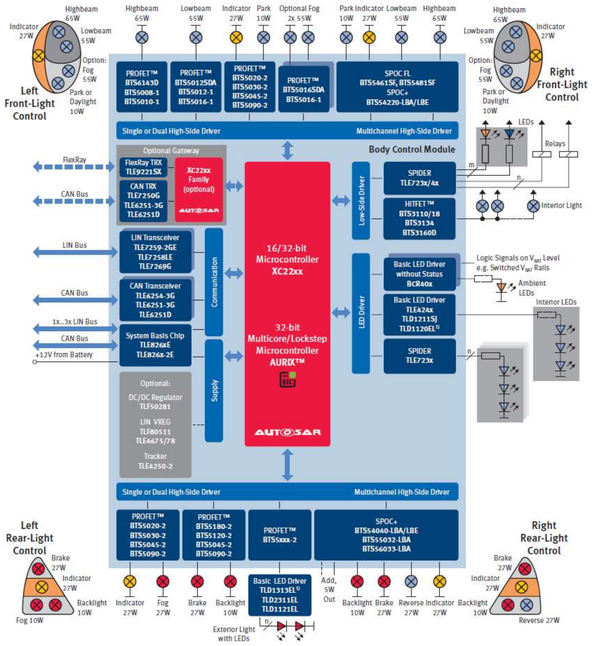
Abstract

- Goal was to design a PMU with reduced footprint at competitive costs and performance
- The target application is an automotive microcontroller system in 40nm CMOS technology with multiple power domains
- This work is a pre-study for next generation fully integrated power management systems for automotive applications

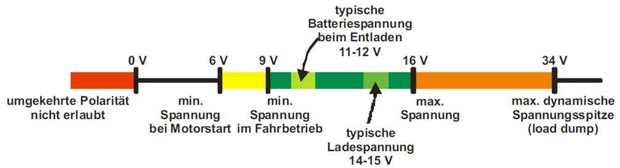
Automotive Applications

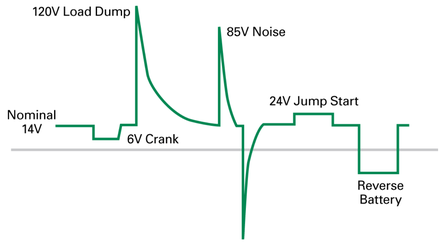


Body Applications



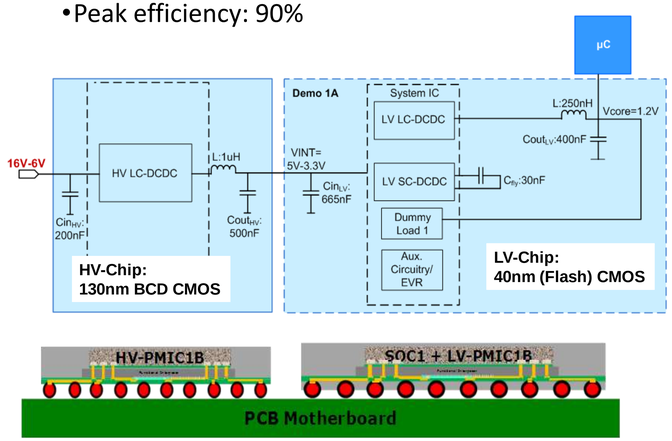
Board Supply in a Car



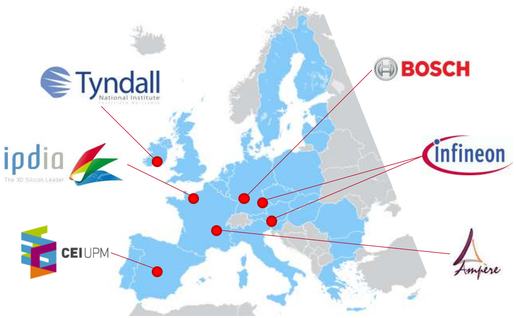


Demonstrator

- High Voltage Pre-Regulator:
  - Vin: 16V…6V
  - Vout: 5V/3.3V
  - $Iload_{max}$: 500mA
  - Peak efficiency: 80%
- Low Voltage Regulators
  - Vin: 5V/3.3V
  - Vout: 1.2V/1.3V
  - $Iload_{max}$: 500mA/200mA
  - Peak efficiency: 90%



Project Partners



- IFAT: Chip Design
- Lyon: Chip Design
- IFAG: Packaging
- Tyndall: Power Inductor, Consortium Lead
- IPDiA: Capacitors & Interposer
- UPM: Concept
- Bosch: Application & Requirements

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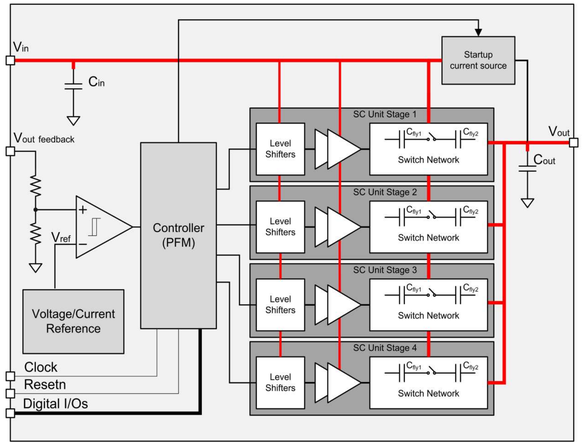
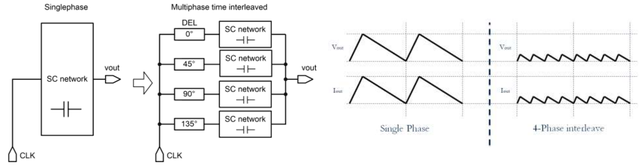
SC DC-DC



- SC DC-DC Converter:
  - 40nm CMOS Technology
  - Series-Parallel
  - Cfly: 8x30nF
  - Cout: 260nF
  - Vout: 1.2V/1.3V
- Gain modes:
  - 1/2 (Vdd=3.3V)
  - 1/3 (Vdd=5V)
- 4 Interleaved Stages:
  - 2 Cfly/stage
  - 9 Switches/stage

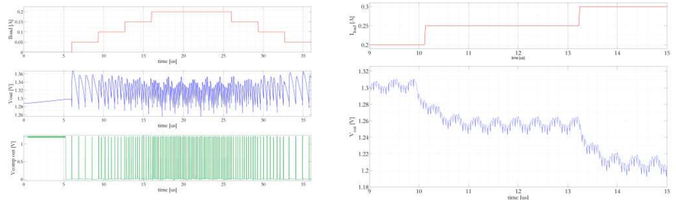
  fsw = 2.5 MHz
- Controller:
  - Pulse Frequency Modulation

Multi Phase Topology



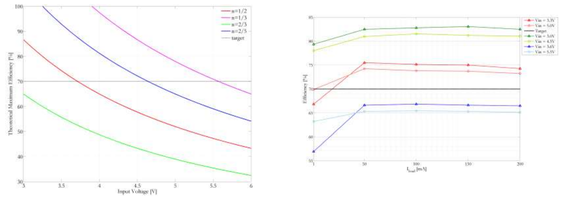
- Multi-phase
  - limits output voltage ripple
  - limits chip noise (lower current peaks at the input)

Simulation Results



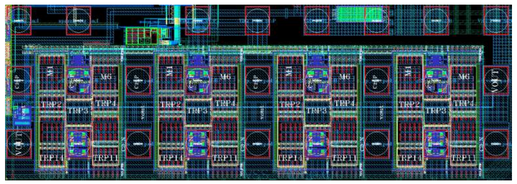
- Driving Capability under Worst Case Conditions (PVT)

Efficiency Simulations

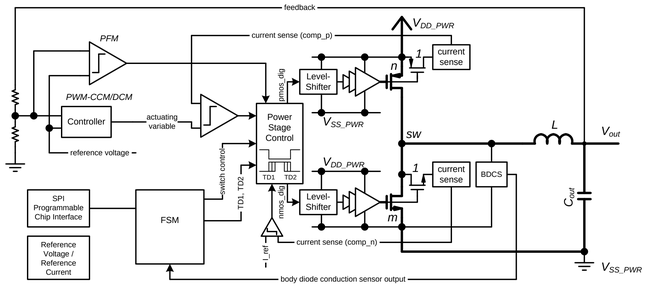


- Simulated Converter Efficiency for Different Input Voltages
- Peak Efficiency at I_{load}=100mA: 84%
- Switching Activity: 20MHz

Layout SC DC-DC



LC DC-DC



- LC DC-DC Buck Converter:
  - 40nm CMOS Technology
  - Vin: 5V/3.3V
  - Vout: 1.2V/1.3V
  - $Iload_{max}$: 500mA
  - fsw: 10MHz
  - Peak efficiency: 90%
- Lout/Cout: 250nH/350nF
- High Side and Low Side Current Sensing
  - Peak Current Control
  - DCM Mode
  - Over Current Protection
- Automatic Dead Time Optimization in the Power Stage
- Operating Modes:
  - PWM-CCM, PWM-DCM, PFM

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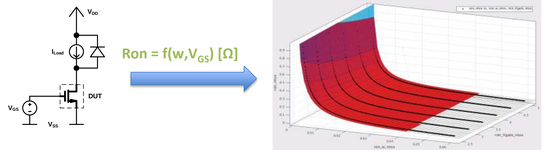
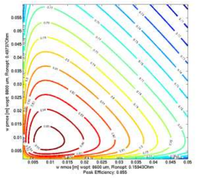
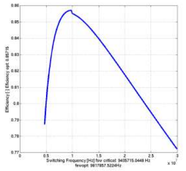
Power Stage Optimization

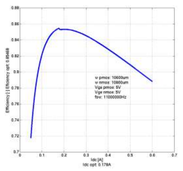
- Device Properties Extracted from Spice Simulations, Optimization is Done in Matlab
- Device Properties: Ron, Turn on Losses, Turn off Losses, Reverse Recovery Losses, Gate Drive Losses, Body Diode Conduction Forward Voltage
- Example Ron:

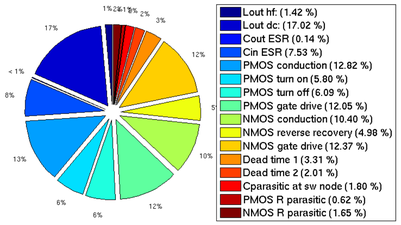


- Optimization Tool

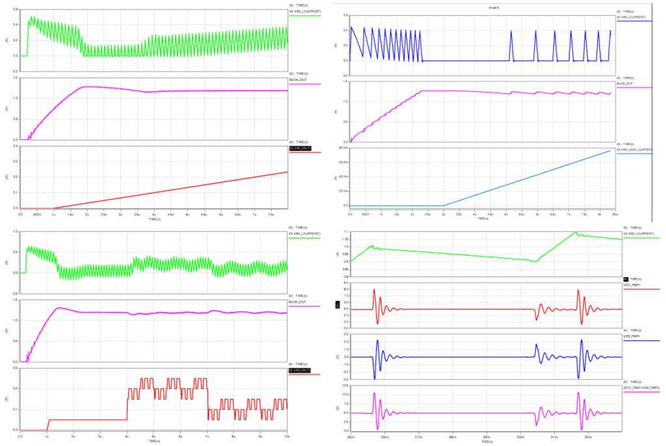




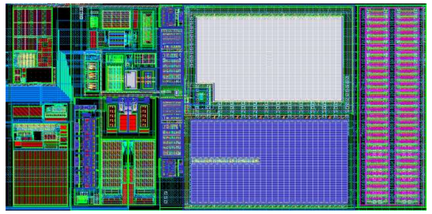




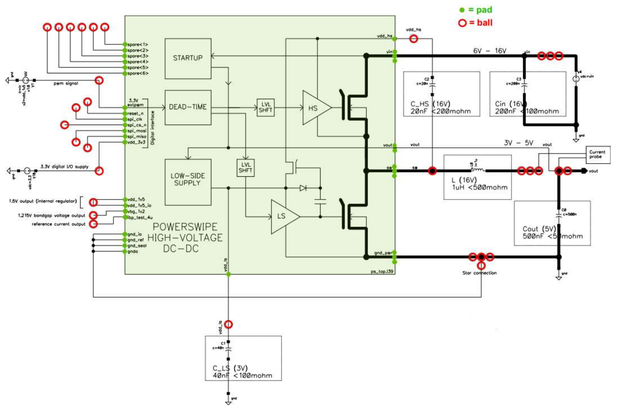
Simulation Results



Layout LV DC-DC

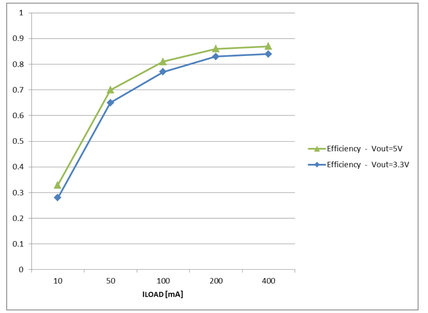


HV DC-DC



- HV DC-DC Buck Converter:
  - 130nm BCD Technology
  - Vin: 6V up to 16V
  - Vout: 5V/3.3V
  - $Iload_{max}$: 500mA
  - fsw: 10MHz
  - Peak efficiency: 90%
- Lout/Cout: 1uH/1uF
- Cls = 40nF (capacitor for low-side driver supply)
- Chs = 20nF (bootstrap capacitor for high-side driver)
- Dead Time Optimization
- Operating Modes:
  - PWM-CCM

Simulation Results



Layout HV DC-DC